WHAT IS CLAIMED IS:

1. An apparatus, comprising:

a first voltage plane;

a signal layer on one side of the first voltage plane;

a second voltage plane on the other side of the first voltage plane; and

a floating trace on the signal layer, wherein the floating trace is electrically connected to the second voltage plane.

2. The apparatus of claim 1, wherein the first voltage plane is a power plane and the second voltage plane is a ground plane.

3. The apparatus of claim 1, wherein the first voltage plane is a ground plane and the second voltage plane is a power plane.

4. The apparatus of claim 1, wherein the signal layer includes a plurality of floating traces, each floating trace being (i) electrically connected to the second voltage plane and (ii) not directly connected to other floating traces on the signal layer.

5. The apparatus of claim 1, wherein the floating trace and the second voltage plane are electrically connected via a plated through hole.

6. The apparatus of claim 1, wherein the floating trace is a microstrip line.

7. The apparatus of claim 6, wherein the microstrip line provides impedance damping.

8. The apparatus of claim 6, wherein the microstrip line reduces resonance between the first voltage plane and the second voltage plane.

9. The apparatus of claim 1, wherein the first voltage plane, the signal layer, and the second voltage plane are separated by a dielectric material.

10. The apparatus of claim 1, wherein the apparatus is a printed circuit board.

11. The apparatus of claim 10, wherein the printed circuit board is associated with at least one of: (i) a flip chip ball grid array package model, and (ii) a pin grid array package model.

12. The apparatus of claim 1, further comprising:

a second signal layer.

13. The apparatus of claim 12, further comprising:

a second floating trace on the second signal layer.

14. A method, comprising:

providing a first voltage plane;

providing a signal layer on one side of the first voltage plane;

providing a second voltage plane on the other side of the first voltage plane; and

providing a floating trace on the signal layer, wherein the floating trace is electrically connected to the second voltage plane.

15. The method of claim 14, further comprising:

positioning the floating trace in the signal layer to reduce cross-talk with a neighboring signal line.

16. The method of claim 14, further comprising:

providing a second signal layer; and

providing a second floating trace on the second signal layer.

17. The method of claim 14, wherein providing the floating trace comprising:

providing a microstrip line on the signal layer.

18. A printed circuit board, comprising:

a signal layer including a plurality of microstrip lines that are not electrically connected to each other on the signal layer;

a power plane under the signal layer and separated from the signal layer by a dielectric material;

a ground plane under the power plane and separated from the power plane by the dielectric material,

wherein each of the microstrip lines is (i) electrically connected to the ground plane via a plated through hole passing through the dielectric material and the power plane and (ii) not directly connected to other microstrip lines on the signal layer.

19. The printed circuit board of claim 18, wherein the microstrip lines provide impedance damping and reduce resonance between the power plane and the ground plane.

20. A system, comprising:

a printed circuit board, including:

a first voltage plane,

a signal layer on one side of the first voltage plane,

a second voltage plane on the other side of the first voltage plane, and

a floating trace on the signal layer, wherein the floating trace is electrically connected to the second voltage plane; and

a dynamic random access memory unit coupled to the printed circuit board.

21. The system of claim 20, further comprising:

a processor coupled to the printed circuit board, wherein the processor and dynamic random access memory unit are to exchange information via signal lines on the signal layer.